

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**In re Application of :**

Robert Madge et. al.

Serial No. :

10/020,407

Filed :

December 12, 2001

For :METHOD OF DETECTING
SPATIALLY CORRELATED
VARIATIONS IN A
PARAMETER OF AN
INTEGRATED CIRCUIT DIE§
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§
§**Group Art Unit :**

2822

Examiner :

Trinh, M.

Attv Docket :

71739 (6653) / 01-299

STATUS REQUESTCommissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request a status of the above referenced application. Please mail the status notification to the address stated below.

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Respectfully submitted,



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Reg. No. 33,562

LSI LOGIC
FAX**RECEIVED**
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FEB 05 2004

LSI Logic Corporation
Legal Department - IP
1621 Barber Lane, MS D-106
Milpitas, CA 95035**OFFICIAL**Date February 5, 2004Number of pages including cover sheet 2**To: US PTO****Mail Stop Status Request**

TC 2822

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From: Connie del Castillo**Intellectual Property Paralegal**

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REMARKS:☐ Urgent ☐ For your review ☒ Reply ASAP ☐ Please commentApplication Number: 10/020,407
Filing date: December 12, 2001
First named inventor: Robert Madge et al.
Attorney docket number: 01-299 / 71739(6653)

Transmitted herewith for filing via facsimile:

- Status Request Letter

Pursuant to 37 C.F.R. 1.8, I hereby certify that this correspondence is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date indicated below:

Feb. 5, 2004

Date

Connie del Castillo

Signature

Connie del Castillo

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